REMARKS

At the time the present Office Action was mailed, claims 1-18, 20, 22 and 26-63 were pending in this application. Claims 17, 18, 20, 22, 26-31 and 37-63 have been cancelled from the application in this response, without prejudice to pursuing these claims in a divisional, continuation, continuation-in-part or other application. Claims 1, 10 and 32 have been amended in this response. Accordingly, claims 1-16 and 32-36 are now pending in this application.

In the Office Action mailed July 16, 2003, claims 1-16 and 32-36 were rejected. More specifically, the status of the application in light of this Office Action is as follows:

A. Claims 1, 2, 4-7 and 9 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,723,900 to Kojima et al. ("Kojima");

B. Claims 3, 7, 8, 10-14 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kojima in combination with U.S. Patent No. 6,544,814 to Yasunaga ("Yasunaga");

C. Claims 32-36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kojima and Yasunaga in combination with U.S. Patent No. 6,297,543 to Hong et al. ("Hong"); and

D. Claims 10 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,252,308 to Akram et al. ("Akram").

The undersigned attorney wishes to thank the Examiner for engaging in a telephone conference on October 2, 2003. During that telephone conference, the present Office Action, the cited references, the pending claims, and several proposed claim amendments were discussed. The following remarks summarize and expand upon the points discussed during the October 2 telephone conference.

A. Response to the Section 102(b) Rejection over Kojima

Claims 1, 2, 4-7 and 9 were rejected under 35 U.S.C. § 102(b) as being anticipated by Kojima.

1. Claim 1 is Directed to a Method of Packaging a Substrate Including Exposing a Portion of a Surface of the Substrate with the Thickness of the Substrate Remaining Approximately the Same

Claim 1 is directed to a method for packaging a microelectronic substrate including disposing an encapsulating material in direct contact with a surface of the microelectronic substrate. The method further includes exposing at least a portion of the surface of the microelectronic substrate by removing a portion of the encapsulating material in direct contact with the surface of the microelectronic substrate. The thickness of the microelectronic substrate remains at least approximately the same before and after the portion of the surface is exposed. The microelectronic substrate is in an operable condition after the portion of the encapsulating material is removed. An advantage of the method in accordance with claim 1 is that removing a portion of the encapsulating material allows heat to be more effectively and efficiently removed from the microelectronic substrate.

2. Kojima Discloses a Method for Forming a Thin Semiconductor Device Including Grinding the Mold Resin and Semiconductor Chip to Planarize the Rear Surface of the Device

Kojima discloses a method for forming a thin, molded semiconductor device in which the thickness of the device is defined by the thickness of the lead frame. First, a semiconductor chip 13 is coupled to an inner lead 16 of a lead frame 12 such that the chip 13 projects above the lead frame 12 (Kojima, Figure 4G). Next, the semiconductor chip 13 and the inner lead 16 are encapsulated with a resin 14 (Kojima, Figure 4H). "After molding with the resin 14, a rear surface 13a of the semiconductor chip 13 is grounded so as to be flush with the upper surface of the outer lead." (Kojima, col. 13, ll. 59-61; Figure 4I.) Accordingly, the semiconductor chip 13 is thinned to create a planar surface across the outer lead 15 and the rear surface 13a of the chip 13.

3. Kojima Fails to Disclose a Method of Packaging a Substrate Including Exposing a Portion of a Surface of the Substrate With the Thickness of the Substrate Remaining at Least Approximately the Same

Kojima fails to disclose a method of packaging a microelectronic substrate including, *inter alia*, "exposing at least a portion of the surface of the microelectronic substrate . . . with the thickness of the microelectronic substrate remaining at least approximately the same before and after the portion of the surface is exposed," as recited by claim 1. For example, assuming for the sake of argument that the semiconductor chip 13, rear surface 13a, and resin 14 of Kojima correspond at least in part to the microelectronic substrate, surface, and encapsulating material, respectively, recited in claim 1, Kojima fails to disclose "the thickness of the microelectronic substrate remaining at least approximately the same before and after the portion of the surface is exposed." To the contrary, Kojima discloses thinning the semiconductor chip to produce a planar surface across his device. Consequently, Kojima fails to disclose each and every element of claim 1, and in fact expressly teaches away from the elements of claim 1 as described in detail below. Therefore, the Section 102(b) rejection of claim 1 should be withdrawn.

Claims 2, 4-7 and 9 depend from claim 1. Accordingly, the Section 102(b) rejection of these claims should be withdrawn for the reasons discussed above with reference to claim 1 and for the additional features of these claims.

B. Response to the Section 103(a) Rejection over Kojima and Yasunaga

Claims 3, 7, 8, 10-14 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kojima in combination with Yasunaga.

1. Yasunaga Discloses a Method of Manufacturing Packaged Semiconductor Devices

Yasunaga discloses a method of packaging semiconductor chips. First, the semiconductor chips are mounted to the surface of an insulating substrate and electrodes on the chips are electrically connected to conductive patterns on the

substrate. Next, the chips are encapsulated with a transfer mold resin, and electrode balls are formed on the side of the substrate opposite the chips. After forming the balls, a laser cuts through the mold resin and the substrate to dice the semiconductor devices.

2. Kojima and Yasunaga Fail to Disclose or Suggest a Method of Packaging a Substrate Including Exposing a Portion of a Surface of the Substrate with the Thickness of the Substrate Remaining at least Approximately the Same

The combination of Kojima and Yasunaga fails to disclose or suggest a method of packaging a microelectronic substrate including, *inter alia*, "exposing at least a portion of the surface of the microelectronic substrate . . . with the thickness of the microelectronic substrate remaining at least approximately the same before and after the portion of the surface is exposed," as recited by claims 3, 7 and 8. Yasunaga fails to cure the above-noted deficiencies of Kojima to support a rejection under Section 103(a). For example, Yasunaga fails to disclose exposing a portion of a surface of his semiconductor chip. Yasunaga merely discloses dicing encapsulated semiconductor devices with a laser. Therefore, the combination of Kojima and Yasunaga fails to disclose all the elements of claims 3, 7 and 8.

Moreover, one of ordinary skill in the art would not be motivated to modify Kojima's method so that his semiconductor chip has the same thickness before and after the rear surface is exposed because such a modification would thwart the purpose of Kojima's invention. Kojima states "[a]ccording to the present invention, there is provided a resin mold type semiconductor device in which a thickness of the semiconductor device is defined by a thickness of the lead frame." (Kojima, col. 2, ll. 12-15.) Kojima further explains that "since the thickness of the resin mold semiconductor device is defined by the thickness of the lead frame, the resin mold type semiconductor device can be made thin with flat front and rear surfaces." (Kojima, col. 2, ll. 31-35). Accordingly, the purpose of Kojima's invention is to form a semiconductor device in which the thickness of the device is defined by the thickness of the lead frame. If Kojima's method were modified to expose the rear surface of the semiconductor chip without thinning the chip, the semiconductor chip would project above the outer lead

and thus thwart the purpose of Kojima's invention. Consequently, one of ordinary skill in the art would not be motivated to modify Kojima's method to arrive at the features of claims 3, 7 or 8. Therefore, the Section 103(a) rejection of claims 3, 7 and 8 should be withdrawn because (a) the combination of Kojima and Yasunaga fails to disclose all of the elements of these claims and (b) one of ordinary skill in the art would not be motivated to modify Kojima's method to arrive at the claimed features.

Independent claim 10 includes, *inter alia*, features generally similar to those described above with reference to claim 1. Accordingly, the Section 103(a) rejection of this claim should be withdrawn for the reasons discussed above with reference to claims 3, 7 and 8 and for the additional features of claim 10.

Claims 11-14 and 16 depend from claim 10. Accordingly, the Section 103(a) rejection of these claims should be withdrawn for the reasons discussed above with reference to claim 10 and for the additional features of these claims.

C. Response to the Section 103(a) Rejection Over Kojima, Yasunaga, and Hong

Claims 32-36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kojima and Yasunaga in combination with Hong. Independent claim 32 includes, *inter alia*, features generally similar to those described above with reference to claim 1. Accordingly, claim 32 is patentable over Kojima and Yasunaga for the reasons discussed above with reference to claims 1, 3, 7 and 8 and for the additional features of claim 32. Furthermore, Hong fails to cure the above-noted deficiencies of Kojima and Yasunaga as references supporting a *prima facie* case of obviousness under Section 103(a). For example, Hong discloses a semiconductor chip and a plurality of outer leads mounted to the chip and electrically connected to the chip with corresponding metal wires. The semiconductor chip is partially encapsulated with a molding compound and has a heat sink attached to one surface. Accordingly, Hong provides no motivation to modify Kojima's method to "remove at least a portion of the encapsulating material . . . with the overall thickness of the at least partially encapsulated microelectronic substrate and support member remaining at least approximately the

same before and after the encapsulating material is removed," as recited in claim 32. Therefore, the Section 103(a) rejection of claim 32 should be withdrawn.

Claims 33-36 depend from claim 32. Accordingly, the Section 103(a) rejection of these claims should be withdrawn for the reasons discussed above with reference to claim 32 and for the additional features of these claims.

D. Response to the Section 103(a) Rejection Over Akram

Claims 10 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Akram. Akram and the claimed invention were, at the time the invention was made, subject to an obligation of assignment to Micron Technology, Inc. Accordingly, Akram cannot be used as a reference to support a Section 103(a) rejection of the claimed invention. Therefore, the Section 103(a) rejection of claims 10 and 15 should be withdrawn.

E. Conclusion

In light of the foregoing amendments and remarks, all of the pending claims are in condition for allowance. Applicant, therefore, requests reconsideration of the application and an allowance of all pending claims. If the Examiner wishes to discuss the above noted distinctions between the claims and the cited references or any other distinctions, the Examiner is encouraged to contact David Dutcher by telephone. Additionally, if the Examiner notices any informalities in the claims, he is also encouraged to contact David Dutcher to expediently correct any such informalities.

Respectfully submitted,

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